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Patents Form 7/77

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7/77

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Statement of inventorship and of right to grant of a patent

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1.	Your reference	GB920020058GB1
2.	Patent application number *(if you know it)*	0228611.0
3.	Full name of the or of each applicant	INTERNATIONAL BUSINESS MACHINES CORPORATION
4.	Title of invention	SEMICONDUCTOR TYPE TWO PHASE LOCKED LOOP FILTER
5.	State how the applicant(s) derived the right from the inventor(s) to be granted a patent	By employment and by agreement
6.	How many, if any, additional Patents Forms 7/77 are attached to this form?	
7.		I/We believe that the person(s) named over the page (and on any extra copies of this form) is/are the inventor(s) of the invention which the above patent application relates to.

Signature

6 December 2002
Date

8.	Name and daytime telephone number of person to contact in the United Kingdom	P Waldner Tel: 01962 816057

Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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(UK resident)
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8393142001

Patents ADP number *(if known)*

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If there are more than three inventors, please write their names and addresses on the back of another Patents Form 7/77 and attach it to this form

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REMINDER

Have you signed the form?

Patents Form 1/77

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Patents Act 1977
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090EC02 E769510-1 D00611
P01/7700 0.00-0228611.0

Request for grant of a patent

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South Wales NP10 8QQ

1.	Your reference	GB920020058GB1
2.	Patent application number *(The Patent Office will fill in this part)*	0228611.0
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	INTERNATIONAL BUSINESS MACHINES CORPORATION Armonk New York 10504 United States of America
	Patents ADP number *(if you know it)*	5196370001
	If the applicant is a corporate body, give the country/state of its incorporation	State of New York United States of America
4.	Title of the invention	SEMICONDUCTOR TYPE TWO PHASE LOCKED LOOP FILTER
5.	Name of your agent *(if you have one)*	P Waldner
	"Address for Service" in the United Kingdom to which all correspondance should be sent *(including the postcode)*	IBM United Kingdom Limited Intellectual Property Department Hursley Park Winchester Hampshire S021 2JN
	Patents ADP number *(if you know it)*	7104417001

6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country	Priority App No *(if you know it)*	Date of filing *(day/month/year)*
7.	If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date or the earlier application	No of earlier application		Date of filing *(day/month/year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*
a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.)

Yes

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	6
Claim(s)	2
Abstract	1
Drawing(s)	2 +2

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	2
Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application

Signature

6 December 2002
Date

12. Name and daytime telephone number of person to contact in the United Kingdom

P Waldner
01962 816057

SEMICONDUCTOR TYPE TWO PHASE LOCKED LOOP FILTER

This invention relates to apparatus for a semiconductor type two phased locked loop (PLL) filter.

BACKGROUND

A Type Two PLL filter system has the well known form shown below in Figure 1. A charge pump circuit operates under the control of a phase/frequency detector to develop a voltage across the filter network formed by resister (R1), and capacitor (C1 and C) which provides the input to a voltage controlled oscillator (VCO). The poles of the filter are set by time constants τ=R1(C1+C2) and τ2=R1C2 and in many applications it is necessary to tune this filter network during operation, for example to compensate for process/operating changes or to change the dynamics of the PLL system during a different mode of operation. When this filter is integrated, this is often performed by changing one of the capacitor values, usually C1. However, C1 is also a parameter in the open loop gain of the PLL and changes in its value often necessitate a change in another of the gain parameters such as the charge pump current to prevent the PLL gain from also changing.

One method of keeping a constant gain is to maintain a fixed relationship between τ1 and τ2 and changing C2 proportionally with C1. This introduces more complexity since it is difficult for C1 to accurately track C2 because of their different bias conditions. A capacitor is relatively easy to adjust within integrated circuit application and can be conveniently formed using a MIS (metal-insulator-semiconductor) or diffused junction structure. A proportion of this capacitance can be controlled by adjusting the bias on this structure which can be done with switching transistors or through some form of continuous control using a linear circuit.

The switching devices are large so as to reduce the parasitic resistance that is introduced. This in turn introduces parasitic capacitances so the design of this arrangement can be difficult.

Furthermore it is problematic to implement capacitors within integrated circuit processes when one side of the capacitor does not connect to ground, that is a floating capacitor. When a capacitor is implemented in this 'floating' configuration, it will normally have a significant parasitic capacitance to ground and occupies a greater silicon area for the same value of capacitance. When implementing switching

devices, these are often also more conveniently configured as switches to ground and so this tends to favour the adjustment of the component at this side of the filter normally combined with C1.

As has already been mentioned in the disclosure, adjusting C1 affects the gain of the PLL system and so normally requires a further secondary adjustment (normally to the charge pump current). Another problem is that adjusting C1 only changes the lower frequency pole $\tau 1$ and usually it would be desirable to change both poles $\tau 1$ and $\tau 2$ simultaneously to maintain a transient response. However, adjustment of the second capacitor C2 is more difficult and often not implemented.

It is desirable to allow the adjustment of both poles simultaneously which avoids the problems of adjusting a single pole only. Retaining a fixed relationship between the two poles in the filter maintains a given transient response for the PLL system.

SUMMARY OF INVENTION

According to a first aspect of the present invention there is provided a semiconductor type two phased locked loop filter having a passive capacitor part and an active resistor part; said active resistor part being integrated with the passive capacitor part.

Integrating an active resistor will apply the same change to both poles and has no effect on the loop gain.

The preferred embodiment describes the active resistor using standard FET devices. The scheme employed also allows continuous control over this component.

The active resistor part may advantageously comprise a transistor.

The active resistor is preferably continuously variable.

The active resistor part is suitably controlled by a resistor regulator circuit operating from a voltage that follows the type two phased locked loop voltage.

The resistor regulator circuit may be bootstrapped to the phased locked loop voltage using a voltage follower configured op-amp.

Advantageously, the resistor regulator circuit comprises a current source and a voltage source.

The current source may be tied to the charge pump current and the voltage source is used to tune the active resistor. The advantage of this is better correspondance in the device current and therefore better matching.

Alternatively the voltage source is suitably tied and the current source is used to tune the active resistor since it is easier to implement a variable current source in CMOS.

Advantageously the passive capacitor part, the active resistor part, the resistor regulator circuit and the voltage follower are all made in the same CMOS manufacturing steps and no special steps for including resistor components is required.

This disclosure describes a scheme for accurately controlling the response of a type two PLL filter system which is particularly suited to on-chip applications using standard CMOS components. By tuning the resistive component using an active component rather than tuning a variable capacitive element or a bank of switching resistors the following advantages result:

(1) only one component needs to be tuned to adjust the filter response whereas with capacitive tuning two parameters would normally need to change to compensate for resulting changes in PLL loop gain;

(2) both of the poles can be tuned simultaneously, with their relative separation remaining fixed since this is set by the ratio of the capacitor values only.

(3) the system uses standard components and only requires a reference current source which will already be available within a PLL system for the charge pump circuit and a voltage reference which is also normally available on a chip containing PLL circuits.

Furthermore the embodiment can provide a silicon area saving over a bank of precise switching resistors or capacitors. Since integrated resistors can be relatively large in area for applications where reasonable accuracy is required, a higher resistor width is needed to minimise photolithographic tolerance. By implication, a high width will result in a proportionally higher length to achieve a given resistor value and so the area of the resistor increases as a square law. High value resistors are also difficult to implement in integrated circuit applications and the scheme described can be particularly beneficial in filter applications which require high values of resistance.

Although the overall area of the active resistor circuitry may be greater than a single passive resistor, using a transistor to implement a resistor is more efficient because the resistive and capacitive parasitic values associated with the transistor will be less than those of the equivalent resistor. In this filter application, the parasitic capacitance down to ground is probably the most important and can make high values of resistance impractical since the effect of the resistor's parasitic capacitance upsets the filter performance.

The filter network is also often the most sensitive area of the PLL system for noise sensitivity. Reducing the area of the active components of the filters reduces the sensitivity to noise pick-up from adjacent wiring on the chip. Using a small transistor to implement the resistor can provide an advantage in this respect. Even though more area is required for the control circuitry, this can more easily be made to be less sensitive to external noise sources. This is because it is effectively not part of the PLL feedback system and its transient performance requirements can be much lower than for the main PLL system.

The capacitive part comprises two capacitors in series, a top capacitor connected to the charge pump and the bottom capacitor connected to ground. The active resistor is connected in parallel across the top capacitor.

When the ground-connected capacitor is the larger of the two, then the resistive part is connected across the smaller capacitor (the phased lock loop connected capacitor) as this is the most efficient configuration. Implementing floating capacitors is difficult so it is easier to make the floating capacitor the smaller.

DESCRIPTION OF DRAWINGS

In order to promote a fuller understanding of this and other aspects of the present invention, an embodiment of the invention will now be described, by means of example only, with reference to the accompanying drawings in which:

Figure 1 is a circuit diagram of a standard Type Two phase lock filter; and

Figure 2 is a circuit diagram of the present embodiment of the invention.

DESCRIPTION OF THE EMBODIMENTS

Figure 2 shows the presently preferred embodiment of the present invention with a FET device, T1, being used to implement the active resistor element within a feedback system enabling accurate control of the resistance value. In this arrangement a voltage follower U1 is used to 'bootstrap' a reference FET device, T2, in the feedback control section to the filter voltage which is under the control of a voltage controlled oscillator (VCO). A current reference, Iref, which can be conveniently derived from the same source as that used to define the charge pump current in the PLL system, is used to define a voltage across T2. This voltage is then compared by an op-amp U2 to a reference voltage Vref and a feedback loop formed by U2 controls T2 (and subsequently T1) such that it simulates a resistance set by Vref/Iref. It is possible to control Iref or Vref to achieve continuous control of the resulting resistor value and therefore PLL filter response. This basic scheme can be used in various circuit topologies to implement a Type Two filter. Since capacitor C1 is larger than capacitor C2; it is normally most efficient to have this capacitor connected at the bottom of the filter (normally ground) within chip applications. Ideally the control loop for the resistance controller needs to have a dynamic response which is better then the PLL system so that the resistor value is maintained during changes in the filter voltage, and this can be provided by this system.

Voltage follower U1 is a conventional operational amplifier configured as a feedback circuit. The voltage follower circuit forces one node to follow another while it decouples the nodes from each other. This decouples the control circuitry from the active resistor. U2 is a conventional operational amplifier configured as a comparator. FETs T1 and T2 are configured as a matched pair so the voltages controlled by U2 at their gates are the same and the voltages at their sources (from the charge pump and decoupled by U1) are the same. Consequently the voltage at the drain of T1 will be the same as the voltage at the drain of T2.

PLLs have very wide application within electronic design and Type Two systems are very widespread since they are relatively easy to analyse in terms of control theory and consequently their performance is both well-understood and deterministic. A typical application would be a frequency synthesizer, for example, within a tuning system on a mobile phone handset. As the frequency is changed on the synthesizer then a different dynamic performance may be required which requires a modification to the filter response to, for example, achieve a better response to disturbances on the input signal. An embodiment of the present invention

allows this to be done without affecting the gain of the system which could be undesirable.

CLAIMS

1. A semiconductor Type Two phased locked loop filter having a passive capacitor part and an active resistor part; said active resistor part being integrated with the passive capacitor part.

2. A filter as in claim 1 wherein the active resistor is a standard FET device.

3. A filter as in claim 1 wherein the active resistor is continuously variable.

4. A filter as in claim 1,2 or 3 wherein Type Two phased locked loop filter operates from a voltage and the active resistor part is controlled by a regulator circuit operating from a voltage that follows the type two phased locked loop voltage.

5. A filter as in claim 4 wherein the regulator circuit is bootstrapped to the phased locked loop voltage using a voltage follower configured op-amp.

6. A filter as in claim 4 or 5 wherein the phased locked loop filter has a current and regulator circuit comprises a current source and a voltage source wherein the current source is tied to the phased locked loop filter current and the voltage source is used to tune the active resistor.

7. A filter as in claim 4 or 5 wherein the phased locked loop filter has a current and regulator circuit comprises a current source and a voltage source wherein the voltage source is tied to the phased locked loop voltage and the current source is used to tune the active resistor.

8. A filter as in any of the preceding steps wherein all the parts are made in the same CMOS manufacturing step.

9. A semiconductor phased locked loop system comprising: a charge pump; a voltage controller oscillator and a Type Two filter as described in any one of claims 1 to 8.

10. A method of manufacturing a semicondutor Type Two phased locked loop filter comprising the steps of:

providing a passive capacitor part and an active resistor part; said an active resistor part being integrated with the passive capacitor part.

11. A method as claimed in claim 10 wherein all the parts are made in the same CMOS manufacturing step whereby no special steps for including passive resistor components is required.

ABSTRACT

SEMICONDUCTOR TYPE TWO PHASE LOCKED LOOP FILTER

There is described a semiconductor Type Two phased locked loop filter having a passive capacitor part and a variable active resistor part; said variable active resistor part being integrated with the passive capacitor part. Integrating an active variable resistor will apply the same change to both poles and has no effect on the loop gain. The variable active resistor part is controlled by a resistor regulator circuit operating from a voltage that follows the type two phased locked loop voltage. The resistor regulator circuit is bootstrapped to the phased locked loop voltage using a voltage follower configured op-amp.

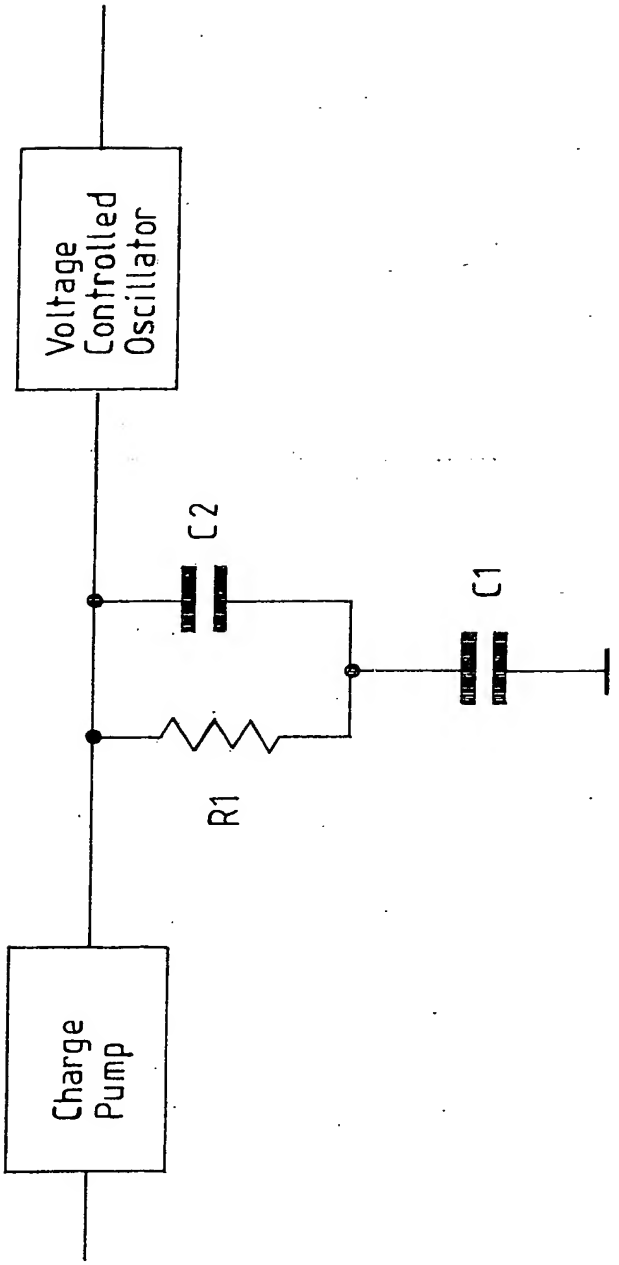

FIG. 1 Type 2 PLL Filter Network

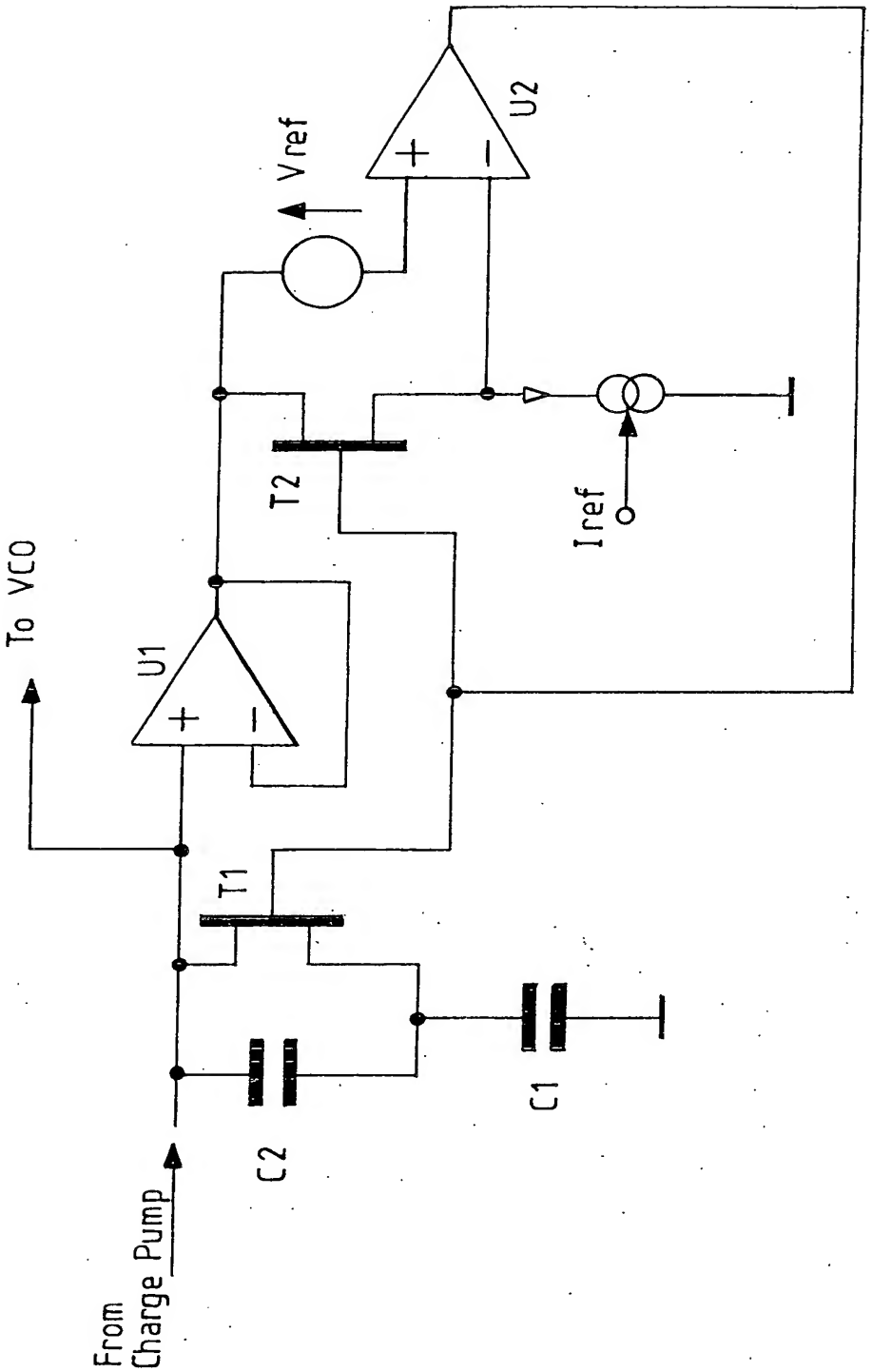

FIG. 2 Filter Control System